Tohoku Forum for Creativity
International Workshop : Spintronics VLSI

Time & Date November 20 (Friday) - November 21 (Saturday), 2015
Venue: Conference Room, Laboratory for Nanoelectronics and Spintronics, Tohoku University

Program:

November 20 (Friday)

	Title	Speaker	Chair
14:00-14:20	**Opening remarks**	Hideo Ohno (Tohoku University)	Tetsuo Endoh (Tohoku University)
14:20-15:00	**Invited talk 1** Low Dissipation Spin-Orbitronics Systems	Kang L Wang (UCLA)	
15:00-15:40	**Invited talk 2** The Progresses of MRAM, the effect on Energy saving, and Discussion on a Potential for Further saving	Hiroaki Yoda (Toshiba)	
15:40-16:10	Group Photo & Break		
16:10-16:50	**Invited talk 3** Fully Functional 64Mb pMTJ STT-MRAM Chips on 300mm Wafers	Yiming Huai (Avalanche)	Tetsuo Endoh (Tohoku University)
16:50-17:30	**Invited talk 4** Recent advances of STT-MRAM for emerging memory Devices	Sechung Oh (Samsung)	

November 21 (Saturday)

	Title	Speaker	Chair
10:30-11:10	**Invited talk 5** Overview of embedded SRAM/DRAM, and prospect of STT-MRAM technology for advanced SoC solutions	Koji Nii (Renesas Electronics)	Takahiro Hanyu (Tohoku University)
11:10-11:50	**Invited talk 6** Emergence of STT-MRAM as a Unified Embedded Memory for Internet-of-Things	Seung H. Kang (Qualcomm)	
11:50-14:00	Lunch		
14:00-14:40	**Invited talk 7** High-Density and Low-Power Applications of Spintronics Circuits: High-Density 1T1MTJ-MRAM Array Design, and Low-Power 4T2MTJ-MRAM-based Pattern Recognition Processor	Hiroki Koike (Tohoku University)	Takahiro Hanyu (Tohoku University)
14:40-15:20	**Invited talk 8** MRAM for hybrid CMOS/Magnetic electronics: perpendicular anisotropy and integrated logic concepts	Ricardo C. Sousa (Spintec)	
15:20-16:00	**Invited talk 9** Spintronics-Based Logic-in-Memory Architecture Towards Dark Silicon Era	Takahiro Hanyu (Tohoku University)	Tetsuo Endoh (Tohoku University)
16:00-16:10	**Closing remarks**	Tetsuo Endoh (Tohoku University)	